

FIG. 1B
(prior art)

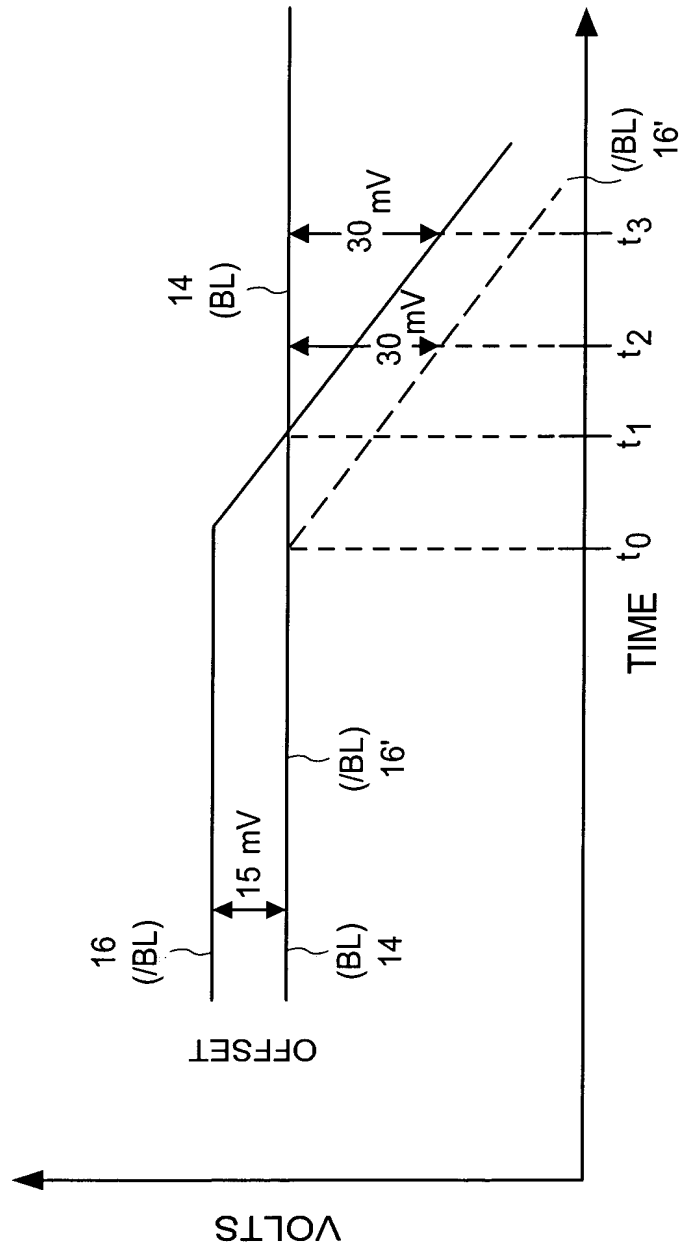


FIG. 1C
 (Prior Art)

Replacement Sheet

Title: MEMORIES HAVING REDUCED BITLINE VOLTAGE OFFSETS

Inventors: Scott T. Becker

Docket No: ARTCP012C

App No: 10/026,245

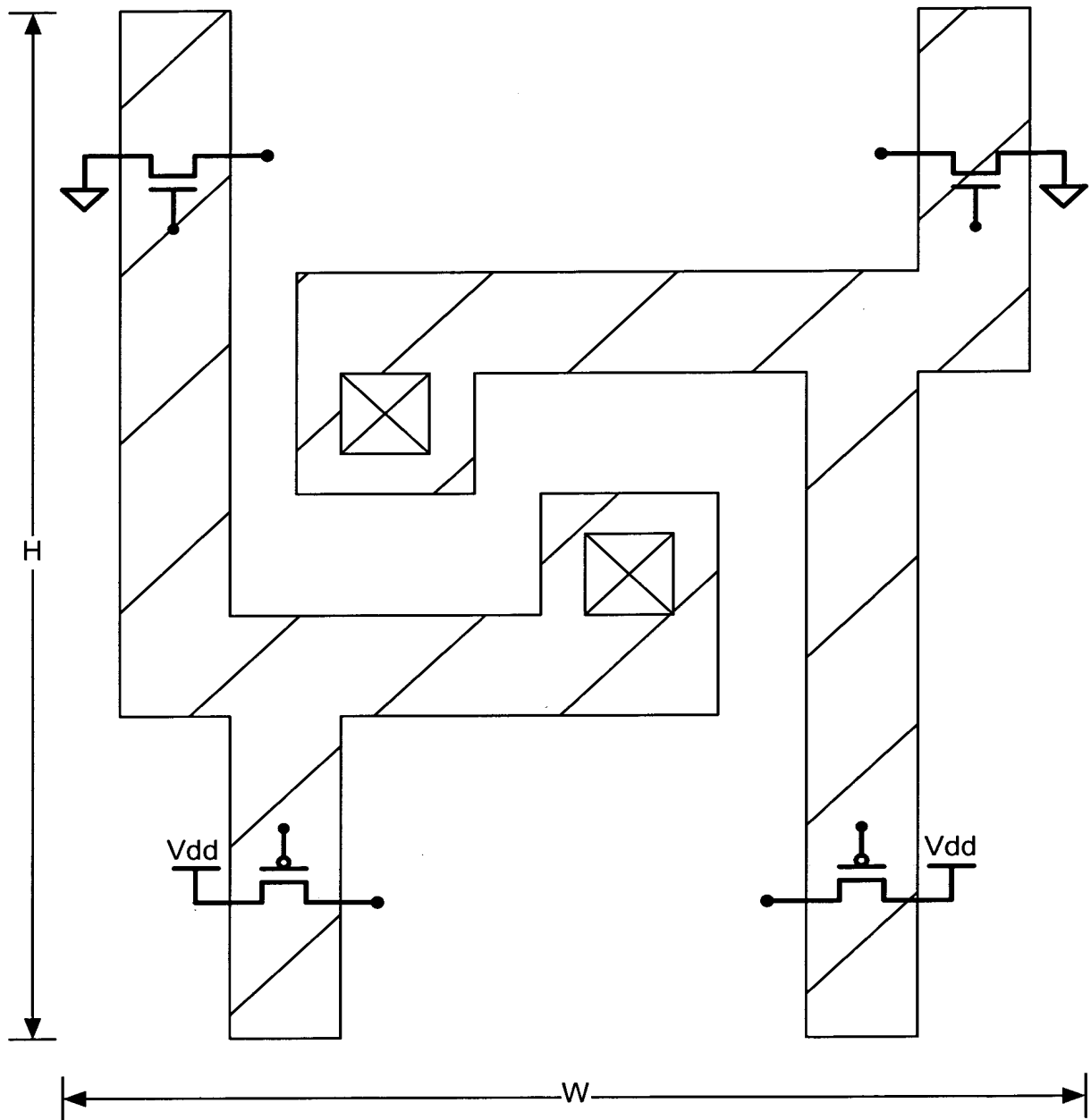


FIG. 1D
(prior art)

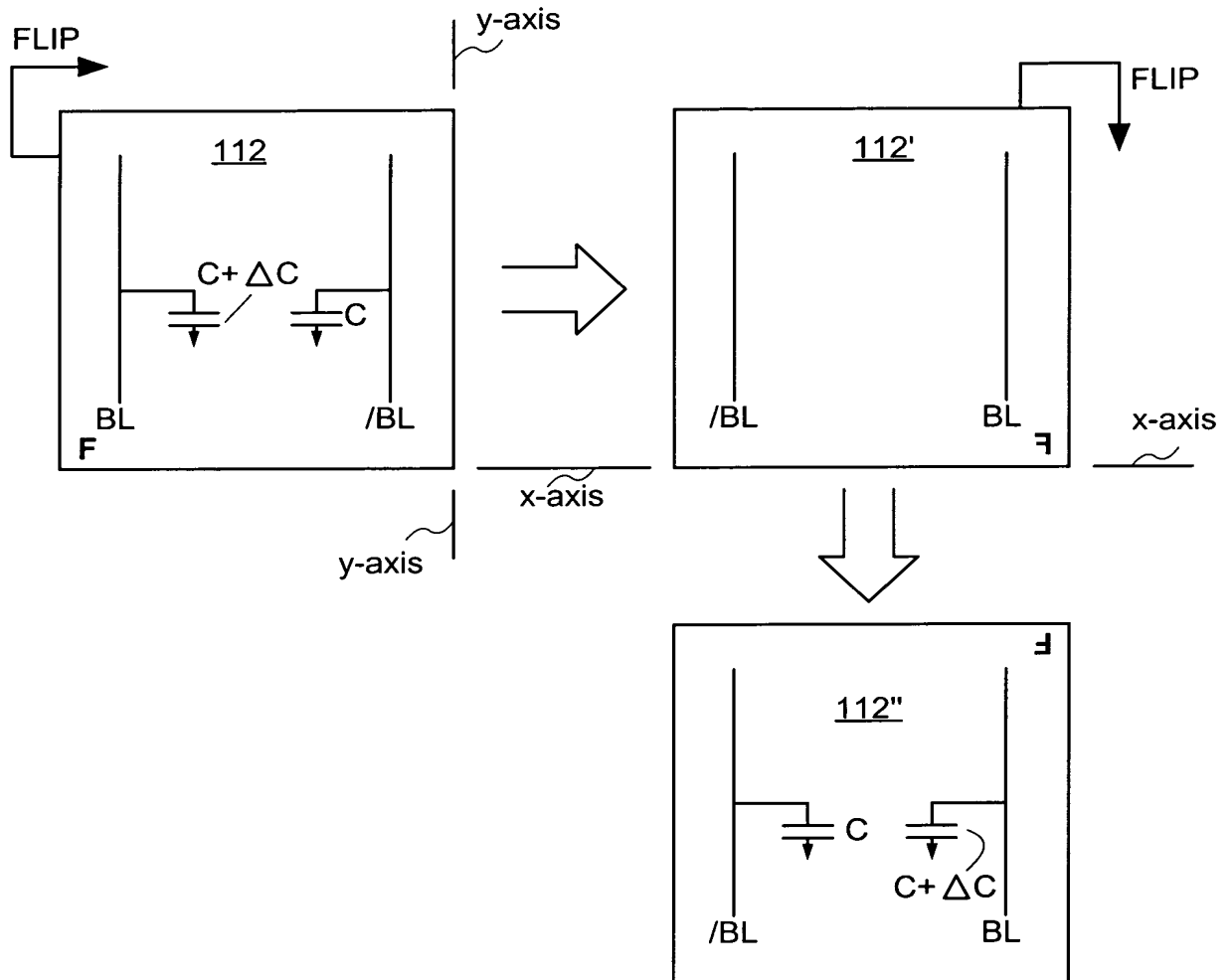


FIG. 2A

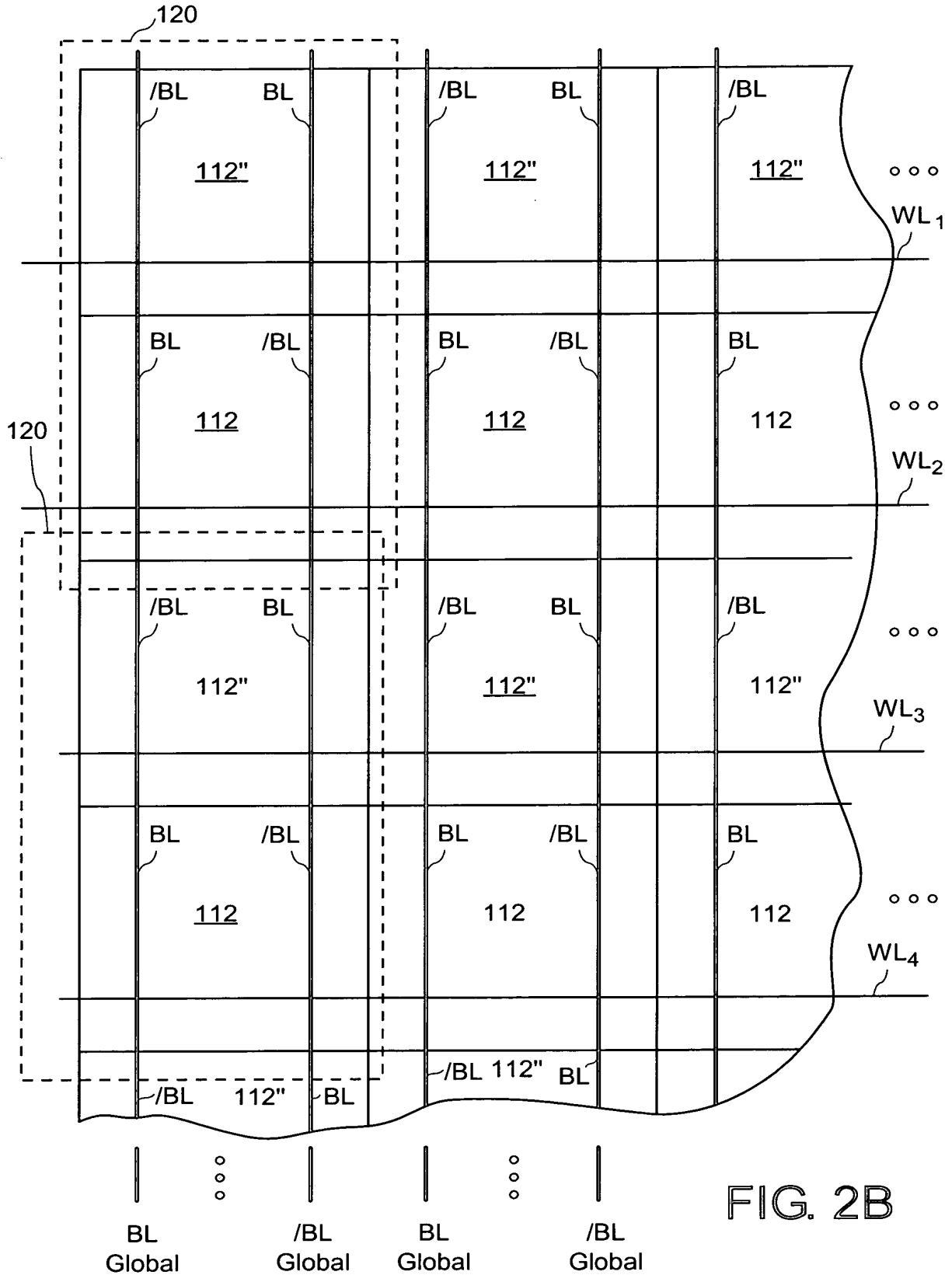
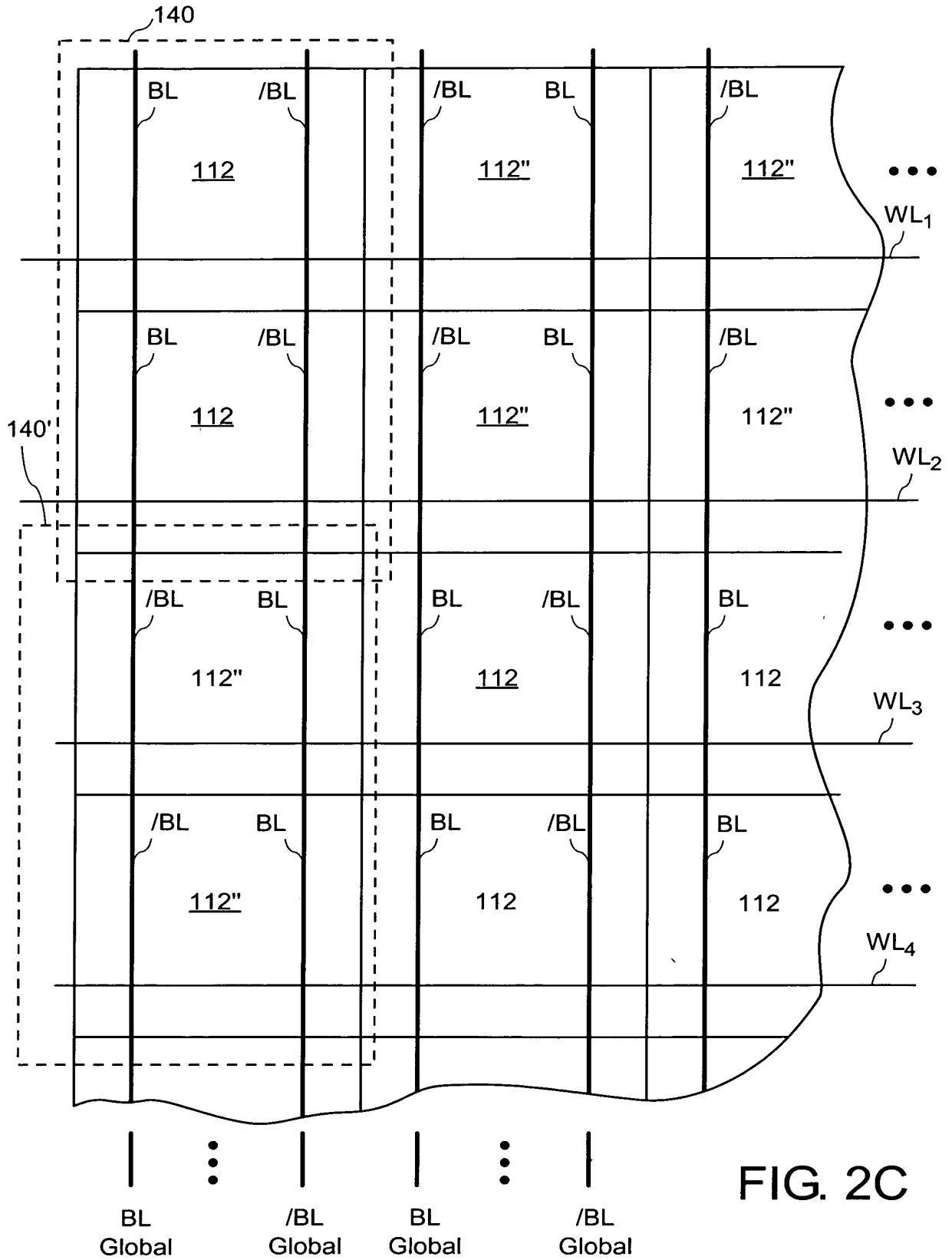


FIG. 2B



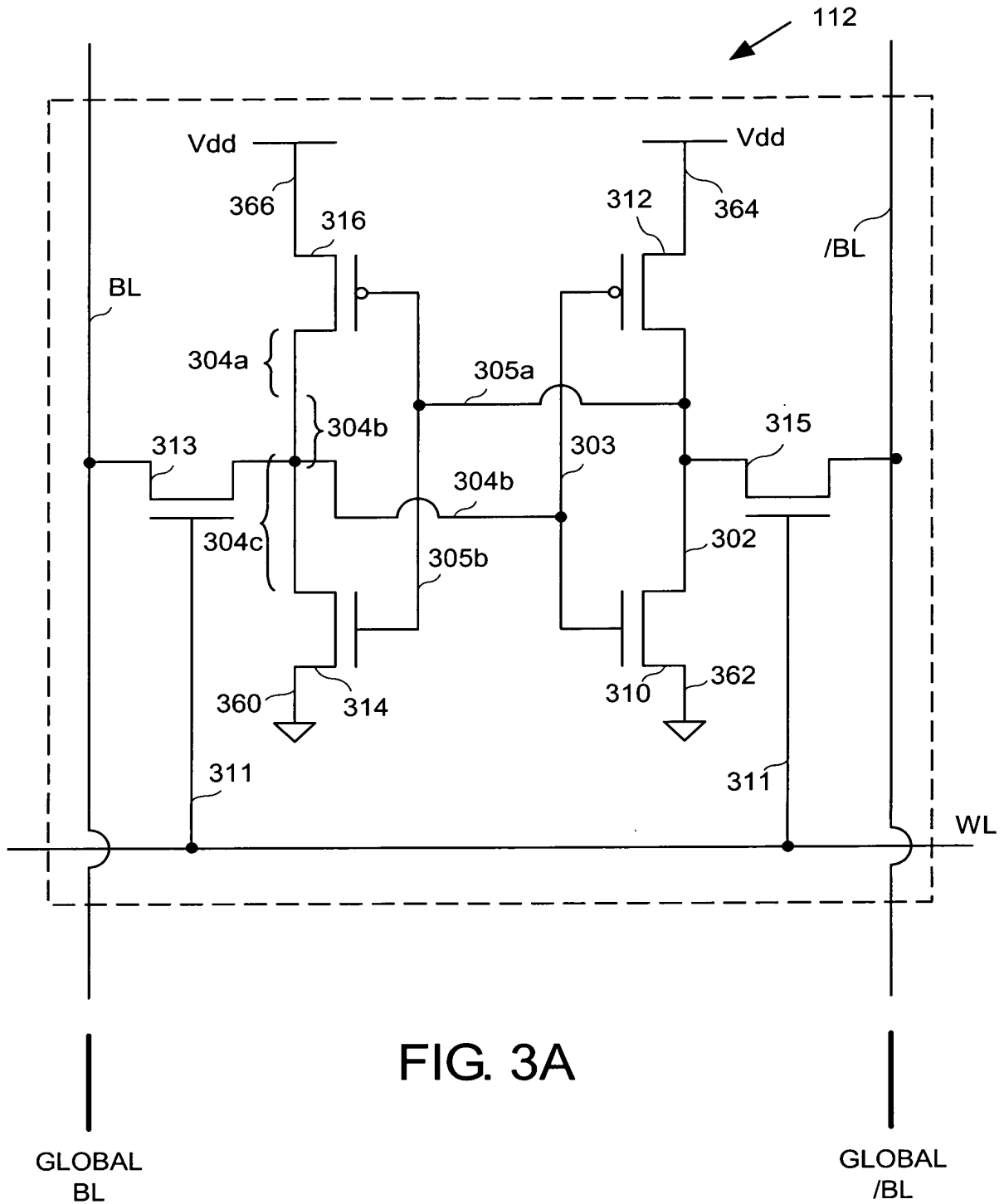


FIG. 3A

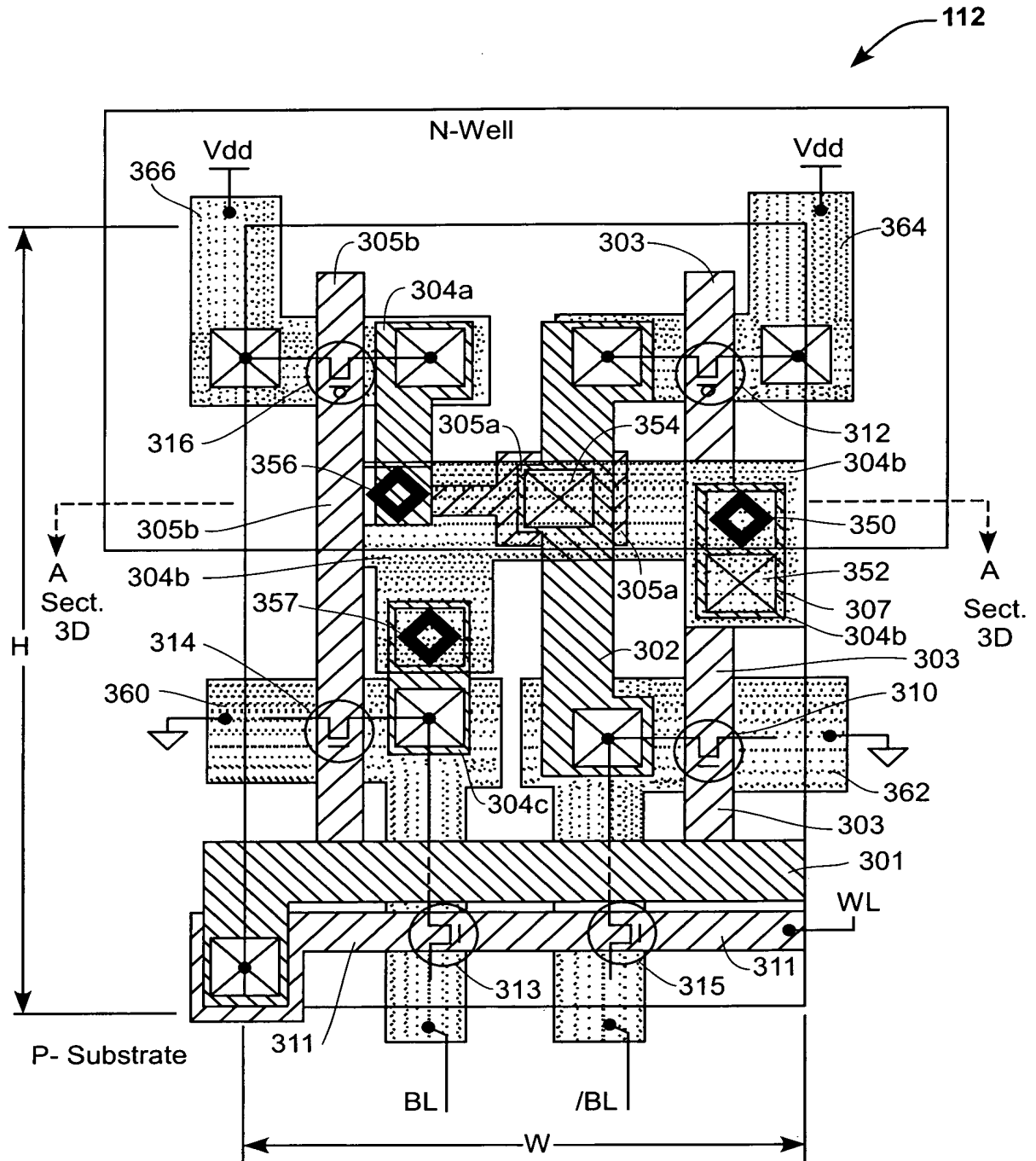


FIG. 3B

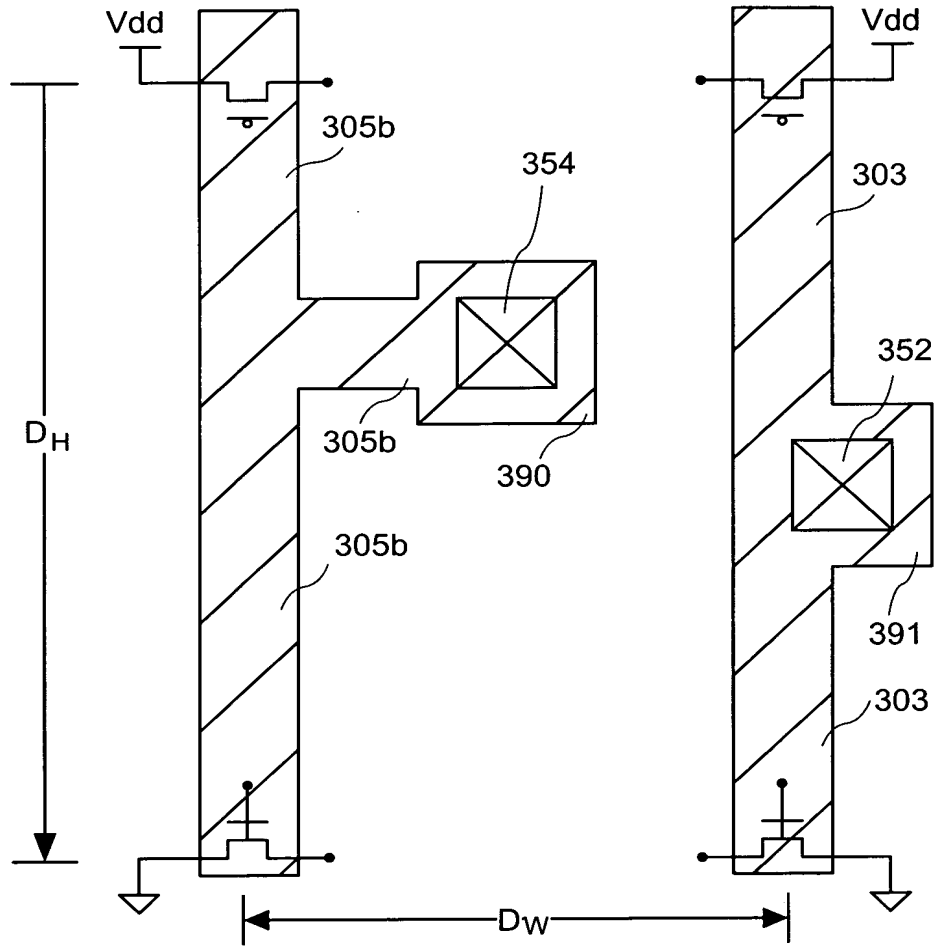


FIG. 3C

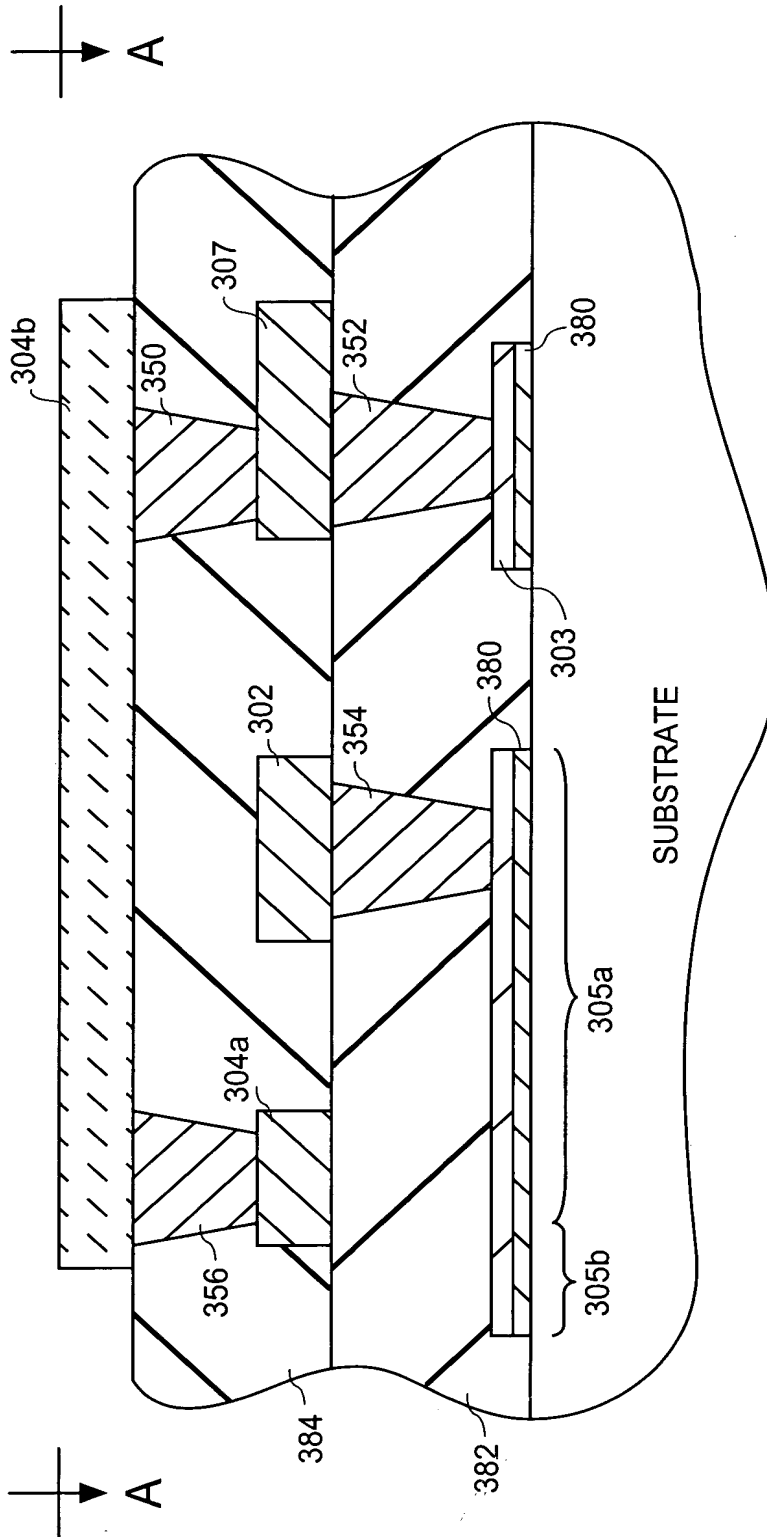


FIG. 3D